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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,049	12/20/2001	Victor Tan Cher 'Khng	00-1117	5617

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 06/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,049	CHER 'KHNG ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18 and 58-64* is/are pending in the application.

4a) Of the above claim(s) *3 and 6-8* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,9-17 and 58-64* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 3 and 6-8 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 4-13-5.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4, 5, 9-11, 13-17 and 58-64 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yew (6137164).

At column 4, line 52 to column 6, line 37; column 7, lines 3-18; and Abbot (6337445), incorporated by reference; column 7, line 33 to column 8, line 67; column 9, line 17-22; column 10, lines 1-12; column 11, lines 16-20 and 38-50, Yew discloses the following:

A semiconductor package comprising: a substrate 420 comprising a first side, an opposing second side, a plurality of die contacts 411, 630 on the first side, and a plurality of bonding sites 634 on the second side in

electrical communication with the die contacts, each bonding site comprising an electrically conductive, bondable metal; a semiconductor die 401 on the first side comprising a plurality of bond pads 633 bonded to the die contacts; and a plurality of external contacts 630 on the second side, each external contact comprising a multi layered metal bump 805 (Abbott) including a first metal layer 801 on a bonding site, a second metal layer 802 on the first metal layer, and a non-oxidizing outer layer 803 on the second metal layer; wherein the die contacts comprise multi layer metal bumps 805; wherein the electrically conductive, bondable metal comprises copper "copper traces having a gold flash," the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer comprises gold; wherein the substrate comprises a material selected from the group consisting of organic polymer materials, epoxy resins "FR-4," and polyimide resins.

A semiconductor package comprising: a substrate having a first side and an opposing second side; a plurality of die contacts on the first side in a pattern, and a plurality of external contacts on the second side in an array in electrical communication with the die contacts, each die contact and each external contact comprising a multi layered metal bump including a base metal layer 801, a bump metal layer 802 and a non-oxidizing outer metal

layer 803; and a semiconductor die flip chip 401 mounted to the first side, the die comprising a plurality of bond pads in the pattern bonded to the die contacts; an encapsulant 450 on the substrate encapsulating the die and the first side; wherein the base metal layer comprises copper, the bump metal layer comprises nickel, and the non-oxidizing outer metal layer comprises gold; an inherent solder mask 450 on the second side inherently configured to electrically insulate the external contacts.

A semiconductor package comprising: a substrate having a first side, and an opposing second side; a plurality of die contacts on the first side comprising first multi layered metal bumps in a pattern having generally planar first tip portions (illustrated in FIG. 6A); a plurality of bonding sites on the second side in an array in electrical communication with the die contacts, each bonding site comprising an electrically conductive, bondable metal 634; a plurality of external contacts on the bonding sites in electrical communication with the die contacts comprising second multi layered metal bumps having generally planar second tip portions (illustrated in FIG. 6A); and a semiconductor die flip chip 401 mounted to the substrate, the die comprising a plurality of bond pads in the pattern bonded to the die contacts; wherein each first multi layered metal bump and each second multi layered metal bump comprises a copper layer 801, a nickel layer 802

and a gold layer 803; an encapsulant 450 on the substrate encapsulating the die; wherein the bonding sites and the external contacts are in a grid array.

An electronic assembly comprising: a supporting substrate 402 comprising a plurality of electrodes 633; at least one semiconductor package on the supporting substrate comprising: a substrate 420 comprising a plurality of bonding sites, each bonding site comprising an electrically conductive, bondable metal; a semiconductor die on the substrate comprising a plurality of bond pads in electrical communication with the bonding sites; and a plurality of external contacts on the bonding sites bonded to the electrodes on the substrate, each external contact comprising a multi layered metal bump including a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing outer layer on the second metal layer; wherein the substrate and the package are configured as a multi chip module; wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer comprises gold; wherein the package further comprises a plurality of die contacts on the substrate in electrical communication with the external contacts, the die contacts comprising multi layer metal bumps bonded to the bond pads on the die.

An electronic assembly comprising: a supporting substrate comprising a plurality of electrodes; and a semiconductor package comprising a substrate having a first side and an opposing second side, a plurality of die contacts on the first side comprising first multi layered metal bumps having generally planar first tip portions, a plurality of bonding sites on the second side in electrical communication with the die contacts comprising an electrically conductive bondable metal, a semiconductor die bonded to the die contacts in a flip chip configuration, and a plurality of external contacts on the bonding sites comprising second multi layer metal bumps having generally planar second tip portions bonded to the electrodes; wherein each die contact comprise a copper layer, a nickel layer and a gold layer; wherein each external contact comprise a copper layer, a nickel layer and a gold layer.

To further clarify the disclosure of an inherent solder mask 450 on the second side inherently configured to electrically insulate the external contacts, it is noted that the language "solder mask" and "to electrically insulate the external contacts" are statements of intended use that do not appear to result in a structural difference between the claimed solder mask and 450. Further, because 450 appears to have the same structure as the claimed solder mask, it appears to be inherently capable of being used for

the intended uses, and the statements of intended use do not patentably distinguish the claimed solder mask from 450. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). In any case, 450 is inherently configured to electrically insulate the external contacts because, as cited, it is disclosed as electrically insulating. Therefore, it inherently electrically insulates the external contacts at least from the space in which it occupies.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes

that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hanoaka (20020030245).

At paragraphs 130, 166 and 201-209, Hanoaka discloses a semiconductor package comprising: a substrate 6 having a first side and an opposing second side; a plurality of die contacts 14 on the first side in a pattern, and a plurality of external contacts 14 on the second side in an array in electrical communication with the die contacts, each die contact and each external contact comprising a multi layered metal bump including a base metal layer, a bump metal layer and a non-oxidizing outer metal layer; and a semiconductor die flip chip 6 mounted to the first side, the die comprising a plurality of bond pads 14 in the pattern bonded to the die contacts; an encapsulant 26 on the substrate encapsulating the die and the first side; wherein the base metal layer comprises copper, the bump metal

layer comprises nickel, and the non-oxidizing outer metal layer comprises gold; wherein each die contact and each external contact is generally pyramidal in shape with a planar tip portion "frustum of a pyramid"; and a solder mask 26 on the second side configured to electrically insulate the external contacts.

To further clarify the disclosure of a base metal layer, a bump metal layer and a non-oxidizing outer metal layer wherein the base metal layer comprises copper, the bump metal layer comprises nickel, and the non-oxidizing outer metal layer comprises gold, as cited, Hanaoka discloses, "as a conductive material for forming the conductive layer 8. [sic] a plurality of different kinds of metals (Ni+Cu or Ni+Au+Cu, for example) may be used. Thereby, the conductive layer 8 may be formed of multiple layers." Hence, Hanaoka discloses the range of three metal layers: Ni, Au and Cu, in any order, and this range includes the claimed embodiment. Therefore, the range of Hanaoka anticipates the claimed embodiment.

Applicant's remarks filed 12-13-4 and 4-13-5 have been fully considered and are moot in view of the new grounds of rejection.

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR:
Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
17-Jun-05